

<b>Notice of References Cited</b>	Application/Control No. 10/038,311	Applicant(s)/Patent Under Reexamination RICH ET AL.	
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-2003/0125918 A1	07-2003	Rich et al.	703/14
	C	US-			
	D	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

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	U	IEEE Standard 1497-2001. "IEEE Standard for Standard Delay Format (SDF) for the Electronic Design Process." Approved Dec.5, 2001.
	V	Open Verilog International . "Standard Delay Format Specification Version 2.1". February 1994.
	W	Open Verilog International . "Standard Delay Format Specification Version 3.0". May 1995.
	X	IEEE DASC Standard Delay Format (SDF). Last modified Dec. 17, 2001. Printed from <a href="http://www.eda.org/sdf/">http://www.eda.org/sdf/</a>

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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	W	Balaji, E. et al. "Modeling ASIC Memories in VHDL." Proc. of EURO-DAC '96. Sept. 16-20, 1996. pp.502-508.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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